16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

#### **DESCRIPTION**

The M5K 4116P and S are 16384-word by 1-bit dynamic RAMs, fabricated with the N-channel silicon-gate MOS process, and ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer poly-silicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities.

#### **FEATURES**

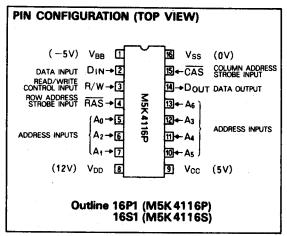
Туре патте	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5K4116P, S-2	150	375	280
M5K4116P, S-3	200	375	280
M5K4116P, S-4	250	410	260

- Standard 16-pin package
- Voltage range on all power supplies

(VDD, VCC, VBB):

±10%

- Low standby power dissipation: 19.8mW (max)
- Low operating power dissipation: 462mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.
- Early-write operation gives common I/O capability.
- Read-modify-write, RAS-only refresh, and page-mode, capabilities
- All input terminals have low input capacitance and are directly TTL-compatible.
- Output is three-state and directly TTL-compatible



 Interchangeable with Mostek's MK4116 in both electrical characteristics and pin configuration.

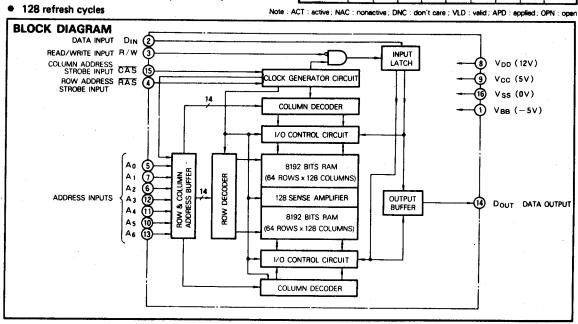
#### **APPLICATION**

Main memory unit for computers

#### **FUNCTION**

The M5K 4116P and S provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, RAS-only refresh, and delayed-write. The input conditions for each are shown below.

									- •
		Inputs							
Operation	RAS	CAS	R/W	Din	Row	Column	Dout	Re- fresh	Remarks
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Page mo
Write .	ACT	ACT	ACT	· VLD	APD	APD	OPN	YES	is identica except
Read-modify- write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	refresh is
RAS-only refre	h ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	1



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### SUMMARY OF OPERATIONS

#### Addressing

To select one of the 16384 memory cells in the M5K 4116P and S, the 14-bit address signal must be multiplexed into 7 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse (RAS) latches the 7 row-address bits; next, the negative-going edge of the column-address strobe pulse (CAS) latches the 7 column-address bits. Timing of the RAS and CAS clocks can be selected by either of the following two methods:

- 1. The delay time from RAS to CAS td (RAS-CAS) is set between the minimum and maximum values of the limits. In this case, the internal CAS control signals are inhibited almost until td (RAS-CAS) max ('gated CAS' operation). The external CAS signal can be applied with a margin not affecting the on-chip circuit operations e.g. access time, and the address inputs can be easily changed from row address to column address.
- 2. The delay time t<sub>d (RAS-CAS)</sub> is set larger than the maximum value of the limits. In this case the internal inhibition of CAS has already been released, so that the internal CAS control signals are controlled by the externally applied CAS which also controls the access time.

#### **Data Input**

Data to be written into a selected cell is strobed by the later of the two negative transitions of R/W input and CAS input. Thus when the R/W input makes its negative transition prior to CAS input (early write), the data input is strobed by CAS, and the negative transition of CAS is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the R/W input makes its negative transition after CAS, the R/W negative transition is set as the reference point for set-up and hold times.

#### **Data Output Control**

The output of the M5K 4116P and S is in the high-impedance state when  $\overline{\text{CAS}}$  is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until  $\overline{\text{CAS}}$  goes high, irrespective of the condition of  $\overline{\text{RAS}}$  (for a maximum of 10 $\mu$ s).

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K 4116P and S, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the  $\overline{\text{CAS}}$ 

pulse in a read cycle, offer capabilities for a number of applications, as follows.

#### 1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

#### 2. Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time, until the next cycle commences. This enables extremely flexible clock-timing settings for  $\overline{RAS}$  and  $\overline{CAS}$ .

#### 3. Two Methods of Chip Selection

Since the output is not latched,  $\overline{CAS}$  is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that  $\overline{CAS}$  and/or  $\overline{RAS}$  can both be decoded for chip selection.

#### 4. Extended-Page Boundary

By decoding CAS, the page boundary can be extended beyond the 128 column locations in a single chip. In this case, RAS must be applied to all devices.

#### Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of  $\overline{RAS}$ , because once the row address has been strobed,  $\overline{RAS}$  is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

#### Refresh

The refreshing of the dynamic cell matrix is accomplished by performing a memory operation at each of the 128 row-address locations within a 2ms time interval. Any normal memory cycle will perform the refreshing, and RAS-only refresh offers a significant reduction in operating power.

#### **Power Dissipation**

Most of the circuitry in the M5K 4116P and S is dynamic, and most of the power is dissipated when addresses are strobed. Both  $\overline{RAS}$  and  $\overline{CAS}$  are decoded and applied to the M5K 4116P and S as chip-select in the memory system, but if RAS is decoded, all unselected devices go into standby independent of the  $\overline{CAS}$  condition, minimizing system power dissipation.

#### Power Supplies

Although the M5K4116P and S require no particular power-supply sequencing so long as the devices are used within the limits of the absolute maximum ratings, it is recommended that the  $V_{BB}$  supply be applied first and removed last.  $V_{BB}$  should never be more positive than  $V_{SS}$  when power supply is applied to  $V_{DD}$ .

Some eight dummy cycles are necessary after power is applied to the device before memory operation is achieved.

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#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter		Conditions	Limits	Unit
V <sub>DD</sub>	Supply voltage			-0.5~20	V
Vcc	Supply voltage			<b>-0.5∼20</b>	V
Vss	Supply voltage		With respect to VBB	-0.5∼20	V
Vı	Input voltage			-0.5~20	V
Vo	Output voltage			-0.5~20	٧
V <sub>DD</sub>	Supply voltage		No.	-1 ~ 15	٧
Vcc	Supply voltage		With respect to VSS	<b>−1 ~ 15</b>	V
V <sub>BB</sub> -V <sub>SS</sub>	Supply voltage		V <sub>DD</sub> -V <sub>SS</sub> >0	0	V
lo	Output current			50	mA
		M5K4116S	Ta = 25 ℃	1000	mW
Pd	Power dissipation	M5K 4116P	Ta = 25 ℃	700	mW
Topr	Operating free-air temperature range			0~70	3
		M5K4116S		<b>−65</b> ~ 150	r
Tstg	Storage temperature range M5K 4116P			-40 ~ 125	٣

#### **RECOMMENDED OPERATING CONDITIONS** ( $Ta = 0 \sim 70 \, \text{°C}$ , unless otherwise noted. Note 1)

				Unit	
Symbol	Parameter	Min	Nom	Max	Unit
V <sub>DD</sub>	Supply voltage	10.8	12	13.2	٧
Vcc	Supply voltage (Note 2)	4.5	5	5.5	٧
Vss	Supply voltage	. 0	0	0	,V
VBB	Supply voltage	4.5	<b>₹</b> 5	-5.7	٧
VIHI	High-level input voltage, RAS, CAS, R/W	2.7		7	٧
V <sub>1H2</sub>	High-level input voltage, A <sub>0</sub> - A <sub>6</sub> , D <sub>IN</sub>	2.4		7	٧
VIL	Low-level input voltage, all inputs	- 1		0.8	V

Note 1: All voltages with respect to Vss. Apply VBB power supply first, prior to other power supplies, and remove last.

#### **ELECTRICAL CHARACTERISTICS**

 $(Ta = 0 \sim 70 \, \text{°C}, \quad V_{DD} = 12 \, \text{V} \pm 10\%, \quad V_{CC} = 5 \, \text{V} \pm 10\%, \quad V_{SS} = 0 \, \text{V}, \quad -5.7 \, \text{V} \leq V_{BB} \leq -4.5 \, \text{V}, \text{ unless otherwise noted})$ 

		Ţ.,	1	Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	
Voh	High-level output voltage (Note 2)	1 <sub>OH</sub> = -5 mA	2.4		Vcc	V
VoL	Low-level output voltage (Note 2)	I <sub>OL</sub> =4.2 mA	0		0.4	V
loz	Off-state output current	D <sub>OUT</sub> floating 0 V ≤ V <sub>OUT</sub> ≤ 5.5 V	<b>– 10</b>		10	μА
l <sub>1</sub>	Input current	$V_{BB} = -5V$ , $0V \le V_{IN} \le 7V$ All other pins = $0V$	- 10		10	μА
DD1(AV)	Average supply current from VDD, operating	RAS, CAS cycling			35	mΑ
CC1(AV)	Average supply current from V <sub>CC</sub> , operating					
BB1(AV)	Average supply current from VBB, operating (Note 4)	$t_{C(RD)} = t_{C(WR)} = 375 \text{ ns}$			200	μΑ
I DD2	Supply current from Vpp , standby	545	-		1.5	mA
CC2	Supply current from V.cc., standby	RAS = VIH  DOUT = floating	- 10		10	μА
1 <sub>BB2</sub>	Supply current from VBB , standby	DOUT = floating			100	μΑ
DD3(AV)	Average supply current from VDD , refreshing	5-10			27	mA
CC3(AV)	Average supply current from VCC refreshing	RAS cycling CAS = VIH	- 10		10	μА
BB3(AV)	Average supply current from VBB , refreshing	t <sub>C(REF)</sub> = 375ns			200	μА
DD4(AV)	Average supply current from VDD , page mode	515 v 515 andre			27	mA
1004(AV)	Average supply current from VCC , page mode (Note 4)	RAS = VIL, CAS cycling				
BB4 (AV)	Average supply current from VBB , page mode	t <sub>C(PG)</sub> = 225ns			200	μΑ
Ci(AD)	Input capacitance, address inputs	1			5	pF
Ci(DA)	Input capacitance, data input	V <sub>I</sub> = V <sub>SS</sub>			5	pF
Ci(R/W)	Input capacitance, read/write control input	f= 1MHz			7	pF
Ci(RAS)	Input capacitance. RAS input	V <sub>I</sub> =25mVrms			10	pF
Ci(CAS)	Input capacitance, CAS input	1			10	pF
Co	Output capacitance	$V_0 = V_{SS}$ , $f = 1MHz$ , $V_1 = 25mVrms$			.7	pF

Note 3 : Current flowing into an IC is positive; out is negative.

<sup>2 :</sup> The output voltage will swing from V<sub>SS</sub> to V<sub>CC</sub> when output loading current is zero. In standby mode V<sub>CC</sub> may be reduced to V<sub>SS</sub> without affecting refresh operations or data retention, but the V<sub>OH</sub> min specification is not guaranteed in this mode.

<sup>4:</sup> VCC is connected only to the output buffer, so that ICC1 and ICC4 depend upon output loading.

#### MITSUBISHI LSIs

## M5K 4116P,S-2, M5K 4116P,S-3, M5K 4116P,S-4

### 16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

### TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

(Ta = 0 ~ 70°C, V<sub>DD</sub> = 12V ± 10%, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, -5.7V ≤ V<sub>BB</sub> ≤ -4.5V, unless otherwise noted. See notes 5.6, and 7.)

	Parameter	Alternative Symbol	M5K 4116-2 Limits		M5K 4116-3 Limits		M5K4116-4 Limits		Unit
Symbol									
			Min	Max	Min	Max	Min -	Max	
C(REF)	Refresh cycle time	tREF		2		2		2	ms
W(RASH)	RAS high pulse width	t <sub>RP</sub>	100		120		150		ns
W(RASL)	RAS low pulse width	tras	150	10000	200	10000	250	10000	ns
w(CASL)	CAS low pulse width (Note 8)	tcas	100		135		165		ns
h(RAS-CAS)	CAS hold time with respect to RAS	tosh	150		200		250		ns
h(CAS-RAS)	RAS hold time with respect to CAS	t <sub>RSH</sub>	100		135		165		ns
d(RAS-CAS)	Delay time, RAS to CAS (Note 9)	taco	20	50	25	65	35	85	ns
d(CAS-RAS)	Delay time, CAS to RAS	torp	- 20		- 20		<b>– 20</b>		ns
SU(RA-RAS)	Row address setup time with respect to RAS	tasa	0		0		0		ns
SU(CA-CAS)	Column address setup time with respect to CAS	tasc	- 10		- 10		- 10		ns
h(RAS-RA)	Row address hold time with respect to RAS	trah	20		25		35		ns
h(CAS-CA)	Column address hold time with respect to CAS	tcah	45		55		75		ns
h(RAS-CA)	Column address hold time with respect to RAS	t <sub>AR</sub>	95		120		160		ns
THL TLH	Transition time	t <sub>T</sub>	3	35	3	50	. 3	50	ns

- Note 5: After power supply is applied, some eight dummy cycles are required before memory operation is achieved.
  - 6 : The switching characteristics are defined as  $t_{THL}\!=t_{TLH}\!=\!5\text{ns}$  .
  - 7 : Reference levels of input signals are V<sub>1H1 min.</sub>V<sub>1H2 min</sub> and V<sub>1L max</sub>. Reference levels for transition time are also between V<sub>1H1</sub> or V<sub>1H2</sub> and V<sub>1L</sub>.
  - 8: Assumes that td(RAS-CAS) ≥ td(RAS-CAS) max.ff td(RAS-CAS) (RAS-CAS) max.fw(CASL) will be increased by the amount that td(RAS-CAS) has decreased
  - 9: The maximum value of \$\tau\_{(\bar{AAS}-\bar{CAS})}\$ does not define the limit of operation, but is specified as a reference point only; if \$\tau\_{(\bar{AAS}-\bar{CAS})}\$ is greater than the specified \$\tau\_{(\bar{CAS})}\$. The maximum value of \$\tau\_{(\bar{CAS})}\$ are similar to the specified as a reference point only; if \$\tau\_{(\bar{CAS})}\$ is greater than the specified \$\tau\_{(\bar{CAS})}\$.

# SWITCHING CHARACTERISTICS ( $Ta=0\sim70$ °C, $V_{DD}=12V\pm10\%$ , $V_{CC}=5V\pm10\%$ , $V_{SS}=0V$ , $-5.7V\le V_{BB}\le -4.5V$ , unless otherwine Read Cycle

Symbol	Parameter		M5K 4116-2 Limits		M5K 4116-3 Limits		M5K 4116-4 Limits		Unit
		Alternative Symbol							
		Symbol .	Min	Max	Min	Max	Min	Max	
t <sub>c(80)</sub>	Read cycle time	tRC	320		375		4 10		ns
tsu(RD-CAS)	Read set-up time with respect to CAS	tnos	0		0		. 0		ns
th(CAS-RD)	Read hold time with respect to CAS	tron	0		0		0		ns
th(CAS-OUT)	Data-out hold time	toff	0	40	0	50	0	60	ns
ta(CAS)	CAS access time (Note 10)	toac		100		135		165	ns
ta(RAS)	RAS access time (Note 11)	trac		150		200		250	ns

Note 10 : This is the value when td(RAS-CAS) ≥ td(RAS-CAS) max. Test conditions , Load = 2TTL .CL=100pF

#### Write Cycle

		Alternative Symbol	M5K 4116-2 Limits		M5K 4116-3 Limits		M5K4116-4 Limits		Unit
Symbol	Parameter								
-		Sylliod	Min	Max	Min	Max	Min	Max	
t <sub>C</sub> (wa)	Write cycle time	t <sub>RC</sub>	320		375		4 10		ns
tsu(WR-CAS)	Write set-up time with respect to CAS (Note 12)	twcs	- 20		20		20		ns
th(CAS-WR)	Write hold time with respect to CAS	twoH	45		55		75		ns
h(RAS-WR)	Write hold time with respect to RAS	twcn	95		120		160		. ns
th(wn-AAS)	RAS hold time with respect to write	tRWL	50		70		85		ns
lh(WR-CAS)	CAS hold time with respect to write	t <sub>CWL</sub>	50		70		85		ns
t w(wa)	Write pulse width	twp	45		-55		75		ns
Su(DA-CAS)	Data-in setup time with respect to CAS	tos	0		0		0		ns
h(CAS-DA)	Data-in hold time with respect to	toH	.45		55		75		ns
th(RAS-DA)	Data-in hold time with respect to RAS	t <sub>DHR</sub>	95		120		160		กร

<sup>11 :</sup> This is the value when td(RAS-CAS) < td(RAS-CAS) max. When td(RAS-CAS) ≥ td(RAS-CAS) max.

ta(RAS) increases by the amount of increase of td(RAS-CAS). Test conditions: Load = 2TTL. CL=100pF

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#### Read-Write, Read-Modify-Write Cycle

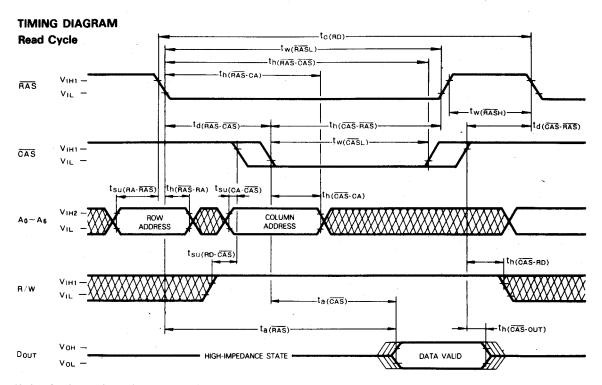
Symbol	Parameter	Alternative symbol	M5K 4116-2 Limits		M5K4116-3 Limits		M5K 4116-4		
							Lim	nits	Unit
			Min	Max	Min	Max	Min	Max	
t <sub>C</sub> (RMW)	Read-modify-write cycle time	t <sub>RWC</sub>	320		405		500		ns
th(wn-RAS)	RAS hold time with respect to write	tawL	50		70		85		ns
th(wn-CAS)	CAS hold time with respect to write	towL	50		70 -		85		ns
tw(wn)	Write pulse width	twp	45		55		75		ns
tsu(RD-CAS)	Read setup time with respect to CAS	t <sub>RCS</sub>	0		0		0		ns
td(RAS-WA)	Delay time, RAS to write (Note 12)	t <sub>RWD</sub>	110		145		175		ns
td(CAS-WR)	Delay time. CAS to write (Note 12)	town	60		80		90		ns
t <sub>su(DA-WR)</sub>	Data-in set-up time with respect to write	t <sub>DS</sub>	0		0		0		ns
th(wR-DA)	Data-in hold time with respect to write	t <sub>DH</sub>	45		55		75		ns
th(CAS-OUT)	Data-out hold time	toff	0	40	. 0	50	0	60	ns
ta(CAS)	CAS access time (Note 10)	toac		100		135		165	ns
ta(RAS)	RAS access time (Note 11)	trac		150		200		250	ns

Note 12: \$\text{\$tsu(\WR-\overline{CAS})} \tau\_{d(\overline{RAS}-\WR)}\$, and \$\text{\$t}\_{d(\overline{CAS}-\WR)}\$ do not define the limits of operation, but are included as electrical characteristics only. When \$\text{\$tsu(\WR-\overline{CAS})} \times \text{\$tsu(\WR-\overline{CAS})}\$ inin. an early-write cycle is performed, and the data output keeps the high-impedance state. When \$\text{\$t}\_{d(\overline{RAS}-\WR)} \times \text{\$t}\_{d(\overline{CAS}-\WR)}\$ min. a read-modify-write cycle is performed, and the data of the selected address will be read out on the data outputs. For all conditions other than those described above the condition of data output is not defined.

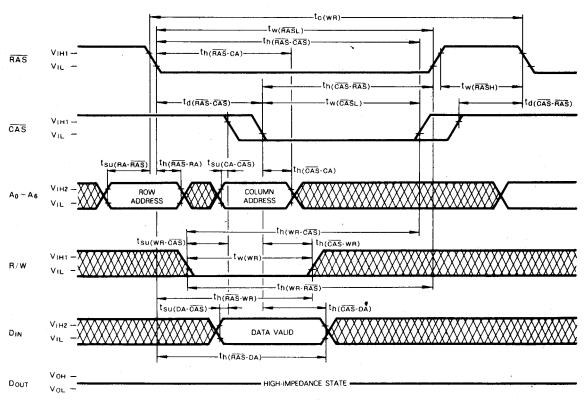
## Page-Mode Cycle

Symbol	Parameter	Alternative symbol	M5K 4116-2 Limits		M5K 4116-3 Limits		M5K4116-4 Limits		Unit
t <sub>C(PG)</sub>	Page-mode cycle time	t <sub>PC</sub>	170		225		275		ns
tw(CASH)	CAS high pulse width	t <sub>CP</sub>	60		80		100		ns

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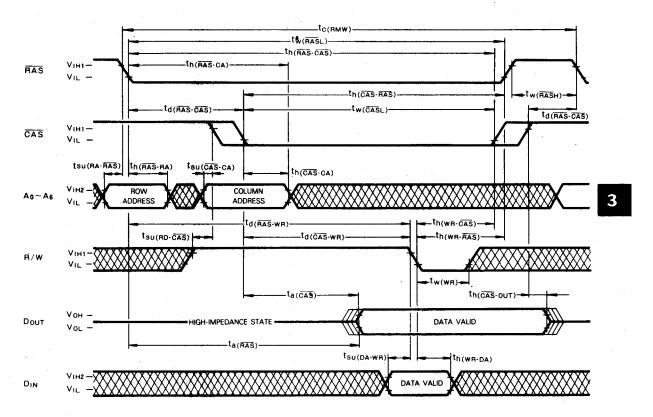


#### Write Cycle (Early Write)

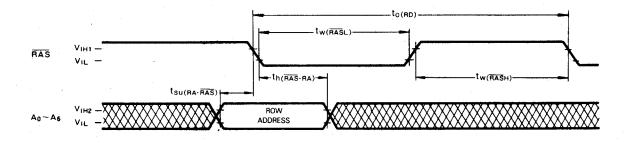


#### 16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

#### Read-Write, Read-Modify-Write Cycle



#### **RAS-Only Refresh Cycle**

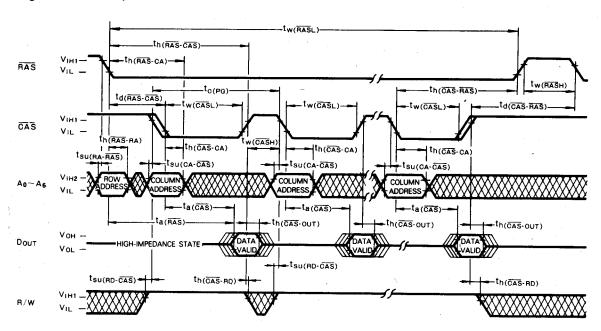


VOH — HIGH-IMPEDANCE STATE

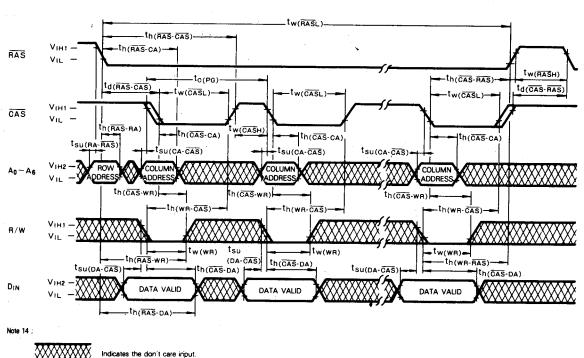
Note 13 :  $\overline{CAS} = V_{1H1}$ , R/W = don't care

### 16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

#### Page-Mode Read Cycle



#### Page-Mode Write Cycle



The center-line indicates the high-impedance state.